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Development of a Circuit Design Model of a Signal Generator of a Payload of a UAV Radio Transmitter based on Auto Compensation of Phase Distortions

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Abstract:

A block diagram of a payload signal generator of a UAV radio transmitter with an autocompensator for phase distortion of a digital computational synthesizer with improved spectral characteristics compared to known solutions is considered. Schematic diagrams of the main paths of the shaper in the Micro-Cap environment have been developed with an analysis of the characteristics of the necessary radio elements and microcircuits. A circuit simulation of the operation of each link of the device in the time domain was carried out. The developed circuit model can be used to design and optimize the characteristics of the signal generator in order to achieve the best performance and the greatest degree of phase distortion compensation.

Keywords: unmanned aerial vehicle, signal generator, digital computing synthesizer, phase distortion autocompensator.

Introduction

The successful operation of unmanned aerial vehicles (UAVs) of various classes and fields of application requires the implementation of a reliable communication channel with the ground control complex [1,2].

The effectiveness of information exchange using UAVs mostly depends on the characteristics of radio transmitters and their signal generation systems, which should provide reliable radio communication both between UAVs and between UAVs and ground control complex [3,4]. It follows from this that the primary task is to optimize the parameters of signal generation systems for data transmission lines, since they contribute to the growth of communication range and the quality of transmission of useful information by choosing the carrier frequency of data transmission, modulation methods, coding and other technical solutions.

One of the methods for improving the spectral characteristics of signal generators of UAV radio transmitters is the method of phase distortion autocompensation, which is implemented by recording distortions using phase detection, subsequent filtering of this signal and amplification. As a result, a compensating signal is formed, which is then used to suppress phase distortions [5-9].

The aim of the work is to develop a circuit model of a signal generator of a UAV radio transmitter with phase distortion autocompensation and its analysis.

Block diagrams of the payload signal generator of the UAV radio transmitter with an autocompensator of phase distortions

The block diagram of the quadrature signal generator is shown in Figure 1. The clock reference generator (CG) should not operate at a frequency higher than 30 MHz for optimal power consumption of the radio transmitter. The diagram shows: FM1 and FM2 are multipliers of the reference clock oscillator, LPF1 and LPF2 are anti-aliasing low-pass output filters for a direct digital synthesizer (DDS), they eliminate side spectral components that are above the clock frequency of the synthesizer in its output spectrum. I and Q are the quadrature outputs of the DDS, QM is the quadrature modulator.

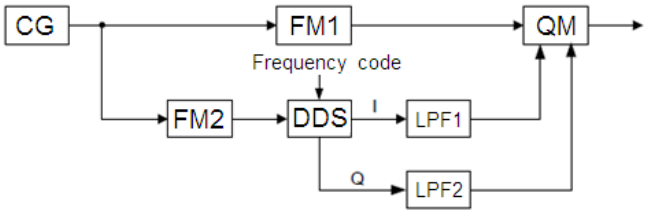

Figure 1 – Block diagram of the quadrature signal generator of the UAV payload radio transmitter

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The disadvantage of this method of formation is the low spectral purity of the synthesized signals, due to discrete side spectral components and the noise part of the DDS spectrum [10-14].

To improve the spectral characteristics of the shapers, it is promising to use a phase distortion autocompensation device (ACPD) of the DDS. The operation of the formation path of the ACPD control signal consists in the isolation of phase distortions of the DDS output signal and their subsequent processing. The block diagram of the ACPD control signal formation path is shown in Fig. 2.

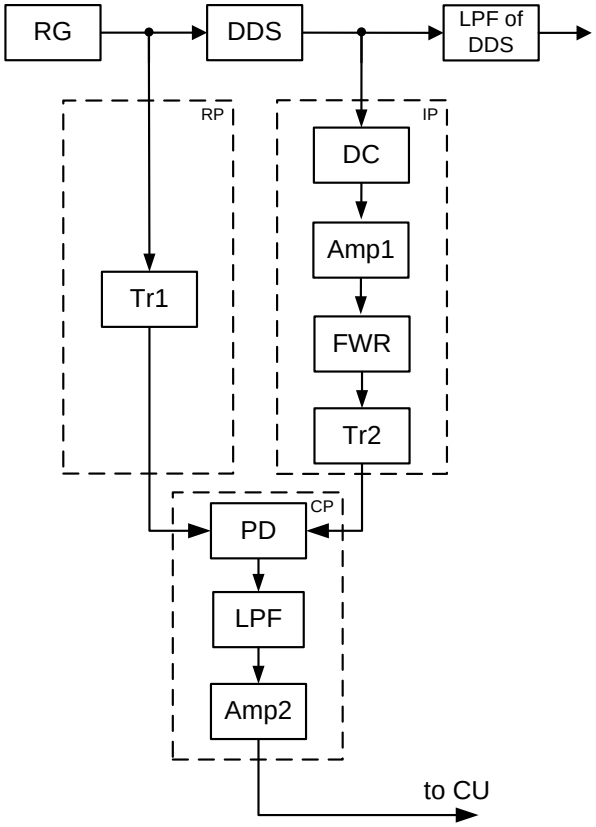

Figure 2 - Block diagram of the ACPD control signal formation path

The following designations are adopted in the scheme: CG - clock generator, DDS - direct digital synthesizer, LPF - low-pass filter, DC - differentiating circuit, Tr - trigger, FWR - full-wave rectifier, PD - phase detector, RP - reference path, IP - information path, CP - control path. The CG signal has the form of a meander, the output signal of the digital-to–analog converter (DAC) of the DDS has a stepped form. Signal processing in the reference and information paths allows to align their shapes and amplitudes while maintaining phase shifts. To do this, the T-trigger Tr1 is used as part of the RP, the differentiating DC, amplifiers A1 and A2, a full-wave rectifier FWR and a similar T-trigger Tr2 are used as part of IP. The phase shift between input signals of the PD is caused by DDS, then this signal is filtered in the LPF and then amplified in A, subsequently the output signal of the device Fig. 2 is used in antiphase to compensate for phase distortions in the control unit (CU).

Since the DDS has two quadrature outputs, it is necessary to compensate for each output signal. To do this, we use a control unit CU made of the two CPSs and a 90-degree phase shifter.

When combining the circuit of the quadrature signal generator (Figure 1) with the circuit of the ACPD control signal generation path (Figure 2), we obtain the circuit of the payload signal generator of the UAV radio transmitter with an autocompensator of phase distortion, shown in Figure 3.

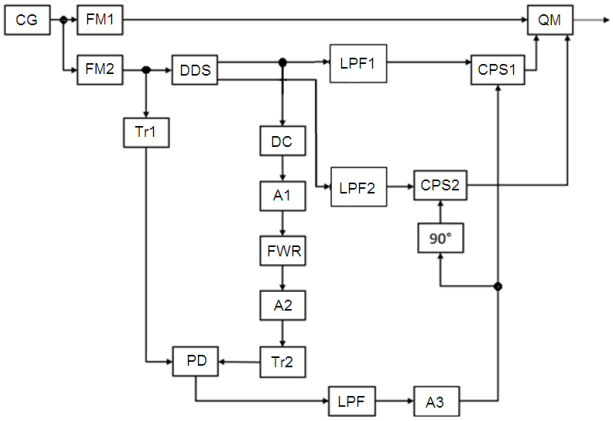

Figure 3 – Block diagram of the payload signal generator of the UAV radio transmitter with an autocompensator of phase distortion

Schematic diagrams of the signal generator

Schematic diagram of the information path

Figure 5 shows the resulting schematic diagram of the information path of the phase distortion autocompensator of the DDS. To tune the developed path in the Micro-Cap program 15,16], a model of a clock generator of rectangular signals with a frequency of 30 MHz and an amplitude of 0.2 V was used as an information signal source.

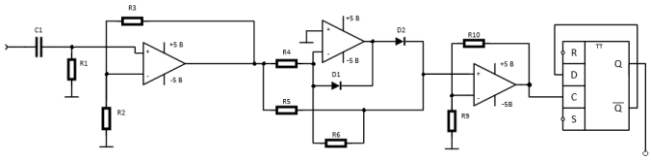

Figure 5 – Schematic diagram of the information path

The schematic diagram of the DC differentiating circuit is a first-order high-pass filter (HFF) with a capacitor C1 of 50 pF and a 1 kOhm resistor with a cut-off frequency set to pass the required clock frequency.

The schematic diagram of the amplifier A1, with a resistor R2 in 0.1 kOhm and R3 in 1 kOhm is implemented on the operational amplifier AD8055. This single-channel voltage feedback amplifier has small errors of differential gain and differential phase not worse than 0.02° at a load of 150 ohms. Due to the wide band (300 MHz), the frequency range with a gain unevenness

within 0.1 dB equal to 40 MHz, the rise rate of 1400 V/ms and the setting time of 20 ns, the component is of interest for a wide range of high-speed circuits. The AD8055 consumes a current of only 5 mA/channel and is fed by bipolar supply voltage of ± 5 V or a unipolar supply voltage of +12 V, while providing a current load capacity of more than 60 mA. These features make the AD8055 an ideal choice for portable equipment and battery-powered devices in which power consumption and dimensions are particularly important.

Schematic diagram of a two-half-period rectifier on one AD8055 operational amplifier, diodes D1 and D2, which are high-speed switching diodes BAS 16L, their features are: high switching speed (less than 4 ns), low leakage current, low capacitance, reverse voltage less than 100 V, small plastic SMD housing. We will take the resistor R4 in 10 kOhm, and R5 = R6 = 5 kOhm.

The circuit of the amplifier A2 is identical to A1 with the only difference that the nominal value of one resistor R10 is assumed to be 0.5 kOhm, and R9 = R2.

The principle model of the T-trigger Tr2 of the reference path of the phase distortion autocompensator DDS is implemented in the Micro-Cap program based on the 74HC74 trigger chip containing two independent D–triggers triggered along the clock signal front at the input C. In terms of input and output signal levels, it is compatible with other standard CMOS logic integrated circuits. The supply voltage range is from 2 to 6 V. The maximum switching time is 6 ns. The signal at the output of Tr2 has the form of a meander.

Schematic diagram of the control path

The schematic diagram of the controlled phase shifter is based on an operational amplifier with resistors R7 and R8 equal to 1 kOhm and a capacitor C2 in 5 UF.

The implementation of the phase detector is based on the logic element “Exclusive OR” on the 74HC86 chip. The input levels of the chip are compatible with standard CMOS levels; with matching resistors are compatible with LS/ALSTTL levels. The supply voltage range is from 2 to 6 V. The maximum switching time is 6 ns.

The low-pass filter of the control path is a first-order RC circuit with the nominals of the capacitor C3 in 5nF and the resistor R11 in 1 kOhm.

The schematic diagram of the amplifier A3 is implemented similarly to A1 and A2 and is a model of an ideal link with a resistor R12 with a resistance of 0.1 kOhm and R13 at 0.2 kOhm.

Figure 6 shows a schematic diagram of the control path of the phase distortion autocompensator of the DDS.

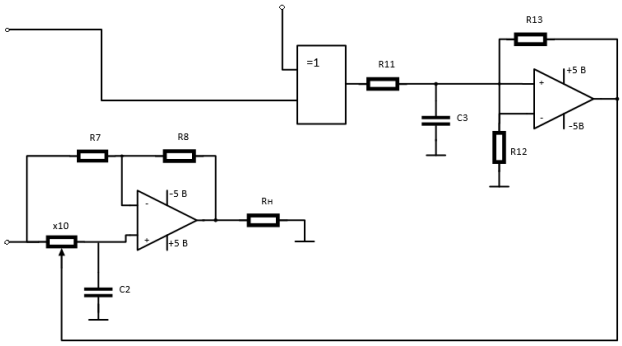

Figure 6 - Schematic diagram of the control path

Simulation of the operation of the signal generator

Using the obtained model of the phase distortion autocompensator of the payload signal generator of the UAV radio transmitter, we will conduct its simulation in the Micro-Cap environment.

Figure 7 shows the waveforms of the signals at the output of the links of the information path.

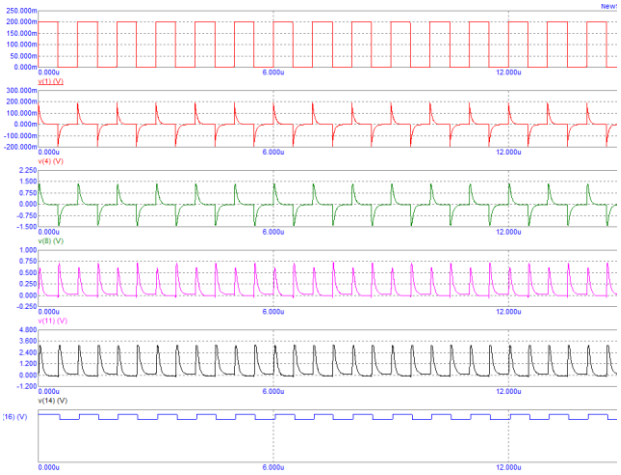

Figure 7 - Waveforms of the signals at the output of the links the information path (from top to bottom): a clock generator CG, a differentiating DC circuit, limiter amplifier A1, full-wave rectifier FWR, amplifier A2 and trigger Tr2

The passage of a signal from the output of a clock generator with an amplitude of 0.2 V and a frequency of 2 MHz through a differentiating circuit is accompanied by the fact that in the time domain the received signal is a sequence of several alternating voltage surges of different polarity. The passage of this signal through A1 is characterized by the fact that in the time domain it is limited to two amplitude values (-1.39 V and 1.39 V). The further passage of the A1 output signal through a full-wave rectifier is accompanied by the fact that negative jumps change their polarity in time, and then it is amplified through the amplifier A2. The passage of the rectified signal through the trigger Tr2 leads to the transformation of its shape to a rectangular one.

Figure 8 shows waveforms of signals at the output of the links of the control path.

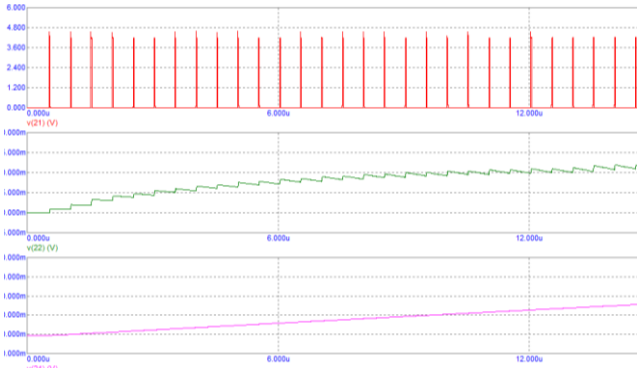

Figure 8 - Waveforms of signals at the output of the control path links (from top to bottom): phase detector FD, low-pass filter LPF2 and amplifier A3

The developed circuit model can be used to design and optimize the characteristics of the signal generator in order to achieve the best performance and the greatest degree of phase distortion compensation.

Conclusion

A block diagram of a quadrature signal generator of a payload of a UAV radio transmitter with an autocompensator of phase distortions of a digital numerical synthesizer is considered. Schematic diagrams and circuit models of the main paths of the shaper in the Micro-Cap circuit modeling program have been developed, taking into account the selection of the necessary radio elements and microcircuits, analysis of their technical characteristics and advantages, and the resulting model of this device has been obtained. The simulation of the operation of each link of the device was carried out to obtain output oscillograms, on the basis of which an analysis of the operation of the autocompensator circuit in the time domain was carried out. The developed circuit model can be used to design and optimize the characteristics of the signal generator in order to achieve the best performance and the greatest degree of phase distortion compensation.

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